ABSTRACT OF THE DISCLOSURE

A method and apparatus for operating a source synchronous receiver. In one embodiment, a source synchronous receiver may include a clock receiver comprising a clock detector and a clock signal buffer. The clock detector may be configured to detect a first clock signal and assert a clock detect signal responsive to detecting the first clock signal. The clock buffer may receive the first clock signal and produce a second clock signal, which may be driven to a digital locked loop (DLL) circuit, where the second clock signal is regenerated and driven to a data buffer of the source synchronous receiver. The clock detect signal may be received by a clock verification circuit. The clock verification circuit may be configured to initiate a reset of the source synchronous receiver upon a failure to receive the clock detect signal. The resetting of the source synchronous receiver may be performed locally, and does not reset the core logic of the device in which it is implemented, nor any other source synchronous port on the device. Thus, other source synchronous ports on the device, as well as the core logic, may be able to continue operations as normal. The method and apparatus may include a source synchronous receiver that is hot-swappable.